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(71) Applicant *(for all designated States except US)*: THE SECRETARY OF STATE FOR DEFENCE IN HER BRITANNIC MAJESTY'S GOVERNMENT OF THE UNITED KINGDOM OF GREAT BRITAIN AND NORTHERN IRELAND [GB/GB]; Whitehall, London SW1 2HB (GB).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)* : SPRACKLEN, Christopher, Timothy [GB/GB]; 47 Ancroft Garth, High Shincliffe, Durham DH1 2UD (GB). SMYTHE, Colin [GB/GB]; 6 Prebends Field, Gilesgate Moor, Durham DH1 1HH (GB).

(74) Agent: BECKHAM, Robert, William; Procurement Executive, Ministry of Defence, Patents 1A(4), Room 2014, Empress State Building, Lillie Road, London SW6 1TR (GB).

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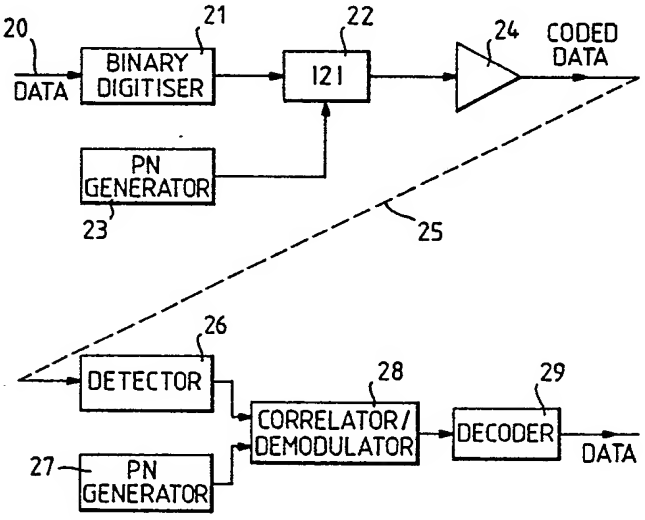

(57) Abstract

A serial data local area network system comprising a serial data highway (10) interconnecting a plurality of transmitting/receiving nodes having transmitters and/or receivers (12) connected thereto characterised in that each transmitter includes means (22), (23) to spread-spectrum modulate digital data signals (21) and address said data signals and means (24) to connect the baseband modulated signal to the highway and each receiver includes means (26)-(29) to selectively demodulate the respective addressed signals from the received signal to reconstitute the data signals, the arrangement being such that multiple simultaneous data signals can be connected to the highway. Direct sequence spread spectrum modulation is preferably employed using a selected code from a family of orthogonal codes. Each code then forms a node or area address, enabling a variety of communications to be achieved eg point-to-point, broadcast, selected area, priority etc. The received signal is oversampled (110), (113) and converted to a binary signal to derive the received sequence and synchronise receiver clocks. Each receiver may include a stack (53) of address codes which are sequentially placed in a sliding polarity correlator (114) through which the received sequence is passed. Means may be provided to change the length of the code sequences in dependence on the number of current users.

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A SERIAL DATA HIGHWAY SYSTEM

The invention relates to digital communications and in particular to serial data local area networks interconnecting multiple nodes.

When information is to be transferred over a multi-node short-haul network parallel channels may be used. For long haul routes, however, the cost would be high and then a serial data highway is used.

Present day local area networks employing coaxial or fibre-optic cable linking the nodes of the network generally operate as time - division multiplex networks. These require each node to transmit at the full medium bandwidth even though the average data rate of a node way be considerably less than the medium bandwidth. In a 100-node Ethernet network, for example, with a medium bandwidth of 10 M bits/sec, data is transmitted from each node at the 10 M bits/sec rate even though the average data rate for a node may be only 10 K bits/sec. Future system bandwidth requirements may be higher than is possible with existing networks. Raw pixel data for example may be required for transmission by such networks so that greater use of graphics may be made. Future demands may also include digital voice transmissions, adding to bandwidth requirements. The system constraint of present networks is the terminal hardware. The transmission medium, ie. the cables, is able to transmit data at many hundreds of megabits/sec. For reasons of cost, size, power consumption and reliability, node hardware is implemented using NMOS or CMOS technology. Assuming that the minimum circuit feature size in the foreseeable future will be $\sim$ 1.5 microns, then the maximum clock rate of these circuits will be $\sim$ 21 MHz. Thus a network should be capable of handling data rates up to this clock rate to have a reasonably long future usefulness.

In addition to bandwidth limitations, present networks do not allow simultaneous use of the network by different nodes. Control of access to the network is required and this leads to communications delays and reliability problems. A central controller may be employed, using a poll - response protocol technique. Reliability of this type of network can be improved by providing a duplicate controller to automatically take over on failure of the

primary unit. Even here, the requirement for a controller is critical to the reliability of the system, particularly for example in a modern warship where survivability depends upon the communications network. Other protocols may be adopted to control access to the medium eg. the node - distributed controller function as in the Litton - DPS system. However, whether a network uses poll-response, token passing or CSMA/CD protocol there is always potentially an access time delay to the network. In a military environment, as in the warship example, network access time could also be critically important and a system allowing instant access to the network would be desirable.

The object of the invention is to provide a serial data highway which overcomes problems associated with current networks.

The invention provides a serial data local area network system comprising a serial data highway interconnecting a plurality of transmitting/receiving nodes having transmitters and/or receivers connected thereto characterised in that each transmitter includes means to spread-spectrum modulate digital data signals and address said data signals and means to connect the baseband modulated signal to the highway and each receiver includes means to selectively demodulate the respective addressed signals from the received signal to reconstitute the data signals, the arrangement being such that multiple simultaneous data signals can be connected to the highway.

Spread-spectrum modulation is known in the radio environment where it is used to make a signal more immune to the effects of noise. In the case of local area networks (LANs) this is not a problem, however the inventors have appreciated that the application of this technique enables many of the above-identified LAN problems to be tackled. By employing a set of different modulation functions to codify each node, a node is allowed immediate access to the network without any danger of contention, can transmit continuously, and at any desired data

rate.

Preferably direct sequence spread spectrum modulation is used where the signal is modulo - 2 added to a pre-determined pseudo-random binary sequence. The data transmission can either be asynchronous with respect to the code sequence clock, or synchronous, in which case the number of data bits transmitted for each sequence period is restricted by the process gain and the system threshold.

At the appropriate receiver a locally generated identical pseudo-random number sequence is synchronised with the incoming spreadspectrum signal to demodulate the transmitted data. Preferably a plurality of orthogonal pseudo-random number sequences is used, each number sequence serving to characterise the required

transmission such that simultaneous transmissions can occur on the network without mutual interference. The orthogonal codes are chosen to have low cross-correlation and high auto-correlation coefficients, the number of psuedo-random bits used to modulate each data bit determining the spreading of the bandwidth of the original signal. Thus the basic principle can be described as Code Division Multiple Access (CDMA), allowing multiple users access to a common medium without fear of contention or access delay.

Preferably the codes are generated by a maximal length code generator (m-sequence). Data bits can be synchonised by detecting the all "1"s state of the m-sequence generator and starting a data bit at that time. A cyclic counter may be used to determine the start of subsequent data bits.

The system can be arranged to operate in a number of modes by appropriate use of different pseudo-random number sequences: each sequence forming a pseudo-random number (pn) code. Thus when used in a point-to-point mode a transmitting node uses the pn code appropriate to a selected destination node. Each receiver in the network is then provided with a correlator programmed to search for the pn code associated with its own address. In order to operate in other modes such as a broadcast mode where a receiver will receive a signal intended for a selected number or all of the users, the receiver is provided with a stack of pn codes and the receiver correlator constantly searches for correlations with the pn codes in the stack. Thus each code in the stack of a particular user represents the source or type of transmitted message which will be accepted.

The correlator output is connected to a demodulator arranged such that when the correlator determines that a transmitted pn code is in phase with one of the locally generated pn codes, the demodulator then decodes the signal data. For this purpose a threshold detector is connected to the correlator output.

Advantageously an adaptive threshold detector is used, the threshold level being adjusted in dependence upon the number of simultaneous spread spectrum signals on the network.

When a coded signal is to be demodulated by a receiver, other simultaneous signals present on the network will appear as random

noise: producing a variable background signal upon which the required binary coded signal is superimposed. Preferably a limiter is provided at the input to the receiver such that a binary signal is presented to the correlator. Advantageously the threshold of the limiter is also adjusted in dependence upon the number of simultaneous spread spectrum signals on the network.

Advantageously the data definition factor - the ratio of the number of simultaneous users to the number of code bits used to define each data bit - is in the range 10^{-4} to 10^{-2}. In addition the signal-to-noise ratio of a single node in the absence of other user should be in the range 7dB to 10dB.

The efficiency of the spread spectrum system can be maximised by making provisions for changing the length of the code sequences used in dependence on the number of active users.

Once correlation with a particular pn code is detected the correlator may be freed to search for other pn codes. When more than one code is received parallel decoding may be adopted or codes may be assigned priorities. The local pn code generator is preferably driven by an accurately controlled frequency source such that once the correlator detects the appropriate incoming pn code, the correlator is no longer required to track the incoming spread-spectrum sequence. The local receiver clock timing may be synchronised with the received spread spectrum signal by oversampling the signal to derive the required timing information. Various codes may be used, for example linear, non-linear, Gold codes, Kronecker sequences, Bent codes, Walsh functions. In addition the length of code may be selected to suit a particular network. For good correlation properties and ease of generation "maximal" length pseudo-noise sequences (m-sequences) are preferably used.

The invention will now be described by way of example only with reference to the accompanying drawings of which:

Figure 1 is a block diagram of a serial data highway;

Figure 2 is a schematic diagram of a spread spectrum serial data highway according to the invention;

Figure 3 shows a shift register generator for a 127-bit m-sequence;

Figure 4 shows in more detail a functional block diagram of a

spread spectrum transmitter;
Figure 5 shows a functional block diagram of a spread spectrum receiver;
Figure 6 illustrates a received signal waveform;
Figure 7a) and 7b) illustrates the sampling used in the determination of the received bit;
Figure 8 is a schematic block diagram of the network including receiver circuits for determining the bit sequences;
Figure 9 is a logical block diagram arrangement of a multi-node spread spectrum local area network (SS LAN);
Figure 10 is a block diagram illustrating in more detail a node control arrangement; and
Figure 11 is a detailed block diagram of a node receiver.

Figure 1 shows a local area network (LAN) comprising a serial data highway 10 having a plurality of nodes 11 to which input/output devices can be added such as the transmitter/receivers (T/R) 12 shown.

Figure 2 is a schematic arrangement of transmitter and receiver to illustrate the basic principle of a serial date highway according to the invention. An input signal 20 for transmission is connected to a digitiser 21, and the digitised output signal is modulo - 2 add (22) to the binary output from a pseudo-random noise (pn) number generator 23. The data thus becomes embedded in a pseudo-random sequence and the narrow band data spectrum signal for transmission. The baseband output from the modulo - 2 adder 22 is connected via a transmitter 24 onto the LAN which may be a screened coaxial cable or a fibre optical cable. The code sequence from the pn generator 23 is selected from one of a family of sequences possessing high auto-correlation and low cross-correlation properties. This sequence can define a unique message address. A remote receiver includes a detector 26 connected to the LAN 25 and a local pn generator 27, producing an identical code sequence to the

transmitter sequence from the pn generator 23. The received signal is continuously correlated to the local pn sequence in a synchroniser/demodulator 28. On acquiring synchronism the outputs from the detector 26 and the local pn generator 27 are compared, bit by bit, to demodulate the embedded data signal. The demodulated digitised signal is then decoded (29) to reconstruct the original signal.

Because of the correlation properties of the selected family of modulation sequences, the receiver synchroniser/demodulator can discriminate between a message which is "addressed" to that receiver

and other simultaneous spread spectrum signals on the network. The spreading of the bandwidth depends upon how many pseudo-random binary digits are used to modulate each data bit and is well known, determines the process gain which is applied at the receiver to discriminate against other signals.

The spread spectrum approach to a local area network is a form of code division multiple access (CDMA) and allows multiple users access to a common medium without fear of contention or access delay. Furthermore, each node is allowed to transmit continuously, if it wishes, at whatever data rate it chooses, rather than having to gather up incoming data into packets for bursting onto the network. The system can be operated in a number of different modes.

a. Point-to-Point Mode.

The pn code used to modulate the incoming data sequence forms the effective 'address' (either source or destination). Consider a particular pn code to be associated with a particular node (although this is, in fact, not the case). In the point-to-point mode, the transmitting node uses a pn code appropriate to the destination node. At the receiver the correlator, which is being used to search for suitable incoming data, will be programmed to look for the pn code that it associates with its own address. In general the system will be arranged such that the correlators of each receiver are continuously searching through a 'stack' of pn codes supplied to them by an associated control unit. These codes constitute the addresses of the incoming messages that the receiver will accept. One of these codes will be the receiver's own code, which it uses to detect incoming point-to-point messages. When the correlator has determined the 'phase' of the incoming pn code in relation to the local pn code generator (if indeed the code is being used on the medium) it passes this information to a demodulator, which then decodes the data and passes it to the control unit (a microprocessor based unit that is arranged to handle higher protocol layers). The correlator is then 'freed' to search for other pn codes (either higher priority messages or messages that may be decoded in parallel). After achieving 'lock' with the local pn code, the correlator is not required to 'track' the incoming sequence since the pn

generators are provided with sufficient frequency stability to maintain lock. Using standard frequency sources it should be possible to keep in synchronism for about 100 data bits however the correlator is arranged to resynchronsie the incoming data every five or so data bits, thereby achieving adequate tracking of the received data.

b. Broadcast Mode.

In broadcast mode a transmitter uses its own associated pn code to modulate the data. This is effectively tagging the data with the source address. Broadcasting is used to transfer data to a number of terminals in parallel, and is used in a situation where the transmitter may not be aware of which receivers wish to accept data of this type. The receivers load their own pn code stack with the addresses of those nodes from which they would like to receive data.

Thus a basic spread spectrum system supports both 'point-to-point' and 'broadcast' type messages. Many other variations are possible, and these will be discussed later.

Spread spectrum techniques are known in the radio environment, however, the conditions applicable to use in a LAN are entirely different. Since each transmitter uses a pn code to modulate the data, the resulting bit stream appears nearly random. Each communications link produces a signal that appears as noise to other simultaneous communications link terminals. In a radio system this noise level is fairly low, unless a transmitter is particular near. Since a spread spectrum is operating in the time domain, it is not possible to 'tune out' such interference as one would in a conventional frequency domain system. This problem is known as the 'near-far' problem and is a particular problem in radio spread spectrum systems. The present invention does not suffer from this problem because all the nodes are connected together by a low loss medium. However the actual signal level of this noise is much higher than in the radio environment, and so the correlation process must be carried out in a high noise environment. A radio spread spectrum system is also subject to man-made and natural interference, often of an impulsive (and hence broadband) nature, as well as narrow-band effects. Because the present invention uses a

screened medium (co-axial or twisted pair) or optical fibres, it is not subject to such effects.

In the arrangement described above, direct sequence modulation is used with the baseband information being added (modulo - 2) to a digital code sequence whose bit rate is much higher than the information signal bandwidth. This results in spreading the signal energy over a bandwidth equal to twice the systems code clock rate. For good correlation properties and ease of generation, 'maximal' length pseudo-noise sequences (m-sequences) may be used. Binary pseudo-noise (pn) sequences (which are also called shift register sequences or m-sequences) are the basis for direct sequence spread spectrum implementation. These imply a deterministic string of binary digits that repeat only after a relatively long period and have statistical properties similar to those of true random numbers. Figure 3 shows a conventional 7-stage (30) shift register generator for a 127 - bit m-sequence with a feedback term formed by the modulo - 2 addition (31) of the first and last stages (D1 and D7). At each clock cycle the contents of the stage are shifted one place to the right. The code at the output 32 is cyclic with a total period 127 times the clock rate. A property of m-sequences which is exploited in the present multiple correlator system is that the modulo-2 addition of a maximal code and a cyclic shift of itself is another replica with a phase shift different from either of the originals.

In a typical LAN there will be a requirement for the code generator 13 to be able to produce a large number of different codes (ie. destination addresses). One approach would be to use a microprocessor simulation of a linear feedback shift register, ie. only exclusive - OR connections appearing in the feedback logic. The contents of the shift register (code sequence) could be stored in one register. The feedback coefficients to each register location could be stored in a second register. When a certain register cell is connected to the exclusive - OR adder, the corresponding feedback bit in the feedback register is set to one, otherwise the feedback word bit contains zero. To calculate the feedback input to the shift register, feedback coefficients must be added with the shift register content, and the number of binary ones

counted. For counting the number of ones a table look-up can be used. The feedback input will be zero for an even number of ones, otherwise one. A successive bit isolation (masking) and exclusive - OR operation may also be used to calculate the feedback input but it can be very time consuming for multi-feedback tap organisations.

Figures 4 illustrates an alternative transmitter arrangement using a parallel implementation to allow fast generation of m-sequences. A high speed RAM 40 stores the current code sequence addresses of users on the network. The RAM 40 is controlled by means of a 68000 microprocessor 41 so as to be able to change the current code sequences, for example by altering code addresses or allocating a new code sequence for a new user added to the network. Address information is connected via input 42 to the microprocessor. This may be system management information or the address for transmission of data. Data for transmission is connected to a buffer 43 which receives sychronising signals from a connection 44 from the microprocessor such that the data can be synchronously added to the appropriate code sequence at the output 45 from the high speed RAM 40. The output 45 is connected to a detector 46 responsive to a selected binary sequence (eg. the all "1"s) which occurs once in the course of a complete cycle of any of the stored m-sequences. The detector 46 produces an output signal which is used to zero a synchronous counter 47 connected to the microprocessor 41. The synchronous counter 47 is used to provide the read out addresses in the high speed RAM 40 and also to provide the source of synchronous pusses for the data stream. The binary data at the output from the buffer 43 are modulo - 2 added (48) to the code sequence.

Parallel implementation of the code sequences allows very fast code generation while still retaining the flexibility to change codes at will. Further address lines of the RAM may be used to select the appropriate sequence. The modulo - 2 addition of code and data is called sequence inversion keying (SIK). This has the effect of inverting the code each time a transition occurs in the data stream. The data transmission described is a synchronous system. It is also possible to use an asynchronous system. The number of data bits that can be transmitted for each sequence period, however, is restricted by the process gain and the system

thresholding. The advantage of using asynchronous data is the resulting simplicity of the transmitter. However asynchronous data bits, random in length, make synchronisation at the receiver more difficult.

Figure 5 illustrates a more detailed receiver for the spread spectrum network. The receiver pn generator 51 is controlled by a microprocessor 52 to generate any of the code sequences currently in use. These current codes are held in a code stack 53. The receiver pn signal is loaded into one serial input 54 of a polarity coincidence correlator 56 and frozen there. The multi-level signal at the receiver node 56 is analysed by an estimator circuit 57 to give an estimate of the number of user signals on the LAN. This number is then used to set the threshold of a hard limiter 58 acting on the received code data connected to a second input 59 to the correlator 55.

The output from the limiter 59 to the correlator 55, which is in binary form, slides past the stationary local sequence with a complete cross correlation being performed at each chip period. When a correlation threshold is passed, as measured by a discriminator 60 connected to the microprocessor 52, the local pn sequence is again shifted through the correlator 55 so as to remain in synchronism with the incoming coded data. If no correlation peak is detected then no signal is transmitted from the discriminator 60 to the input 61 to the microprocessor 52. Then the microprocessor is programmed to assume that the current code sequence is not in use on the network and the following sequence in the code stack 53 is loaded into the correlator 55. Once a correlation peak is detected the coded data and the code sequence pass through the correlator 55 in synchronism to respective inputs of a demodulator 62. The output 63 from the demodulator carries the binary coded data signal which can then be decoded to reconstruct the transmitted message. The conventional problems of initial signal acquisition (or synchronisation) and the subsequent tracking of the signal for demodulation are resolved in the present invention using the digital correlation technique ie a continuous data acquisition is performed in the correlator using the correlation discriminator to indicate signal acquisition.

The invention is baseband in nature but demodulation is carried out by a method known as "integrate and dump". At any time the network may have k simultaneous users. Thus in addition to the signal address to the j'th node (say) there will be (k - 1) other code sequences as well as noise and interference, n(t), separate from the information signals. In the j'th receiver the effect of multiplying the incoming signal by the code representing the j'th node's address is to spectrally spread the received noise and interference so that their energy is spread over a wide bandwidth. The signal is effectively integrated over the bit period and on filtering the signal about the data band-width the desired message signal can be "dumped", providing the family of address codes have the desired auto- and cross-correlation properties. To avoid confusion which may occur when the received signal falls to zero it is preferable to use bipolar signal transmission with a negative voltage signifying a logical "0".

Figure 6 illustrates the form of the multilevel signal that will be received from the network. The signal varies between the limits +nV and -nV where n is the total number of transmitting nodes and V is the signal voltage which may be positive or negative for a logical "1" or "0". At any time t the signal is the sum of the number of nodes transmitting a "1", A(t), and the number of nodes transmitting a "0", -B(t), ignoring the effect of noise.

This scheme is illustrated in Figure 7a) which shows how the correct sequence is recovered from a binary waveform whose sequence rate is correct, but whose phase is non-aligned with the sampling periods. The case illustrated in Figure 7b) is similar to that in a), but the sequence rate is slightly faster than the nominal value, resulting in a phase shift of the recovered sequence, which is nevertheless still correct. Further reference to Figure 8 illustrates the circuit arrangement for sampling and processing the received signal. The transmitted signal 101 formed by the modulo-2 addition (102) of data (103)

and code sequences (104) has added signals from other transmitters 105 as well as noise 106 to produce the composite input signal 107 to the receiver 108. The input signal 107 is sampled by the 1 bit A/D converter 109 at a rate nominally twice the bit rate of the transmitted signal 101. In Figures 7a and 7b sampling is done at times indicated by the vertical lines 110 on an example data sequence "00111100110". In Figure 7a the data period T_1 is exactly twice the sample peried 111 while in Figure 7b the sample period 111 is slightly more than half the data period T_2. The signal samples are collected in groups of three and a majority voting circuit 112 gives the received signal bit which is connected to the input of a sliding polarity coincidence correlator 114. Locally generated code sequences (105) are also placed sequentially into the correlator 114. When a match occurs, the data signal 103 is recovered and dumped into the data sink 116. The sliding polarity coincidence correlator 114 performs a continuous acquisition on the data stream, and so no tracking circuitry is necessary. The correlator works by continuously comparing the local sequence with the input stream and counting the number of agreements (A) or disagreements (D) that occur over the entire sequence length (L). A calculator 117 calculates the value of their difference divided by the sequence length ((A-D)/L). These values are updated each time a new data bit is read in. If the (A-D)/L value exceeds a lower one of a pair of threshold values in a threshold circuit 118, synchronisation is assumed. If the upper threshold is exceeded, then a logical '0' is passed to the data sink. Conversely, a '1' is passed on if the lower threshold boundary is exceeded. This is because of the modulo-2 addition of the sequence and data at the transmitter, resulting in the sequence itself on adding '0' and the sequence's complement on adding '1'.

The reception of data modulated on any other code sequence results in the value of (A-D)/L being within the threshold values and so no data is fed to the correlator. The calculation of this threshold value is dependent on a number of

factors as is discussed elsewhere.

An improvement in the bit error performance of the 1-bit receiver of Figure 8 is possible by increasing the quantisation of the input waveform. Two methods for doing this are possible. The first involves the use of multibit A/D converters. A converter providing n bits of data identifies n^2 signal levels and n parallel correlators are used to correlate the binary signal from the different data bits in the n-bit word. The results from these are then combined, using appropriate weighting factors for the most significant bits, to obtain the data bit. The second method involves the introduction of a dither signal to the received signal, which helps when regulated noise is present on the line. The first method can improve performance by ablut 10-20%, but at great additional complexity and hardware expense. The particular benefits obtained from the second method are obtained with less additional complexity at the receiver.

When a node wishes to transmit, a single code sequence is taken from the code stack according to the type of transmission required eg point-to-point, broadcast or selected receiver groups. The selected code is then used to modulate the data for transmission. Receivers not using the same code sequence will receive a signal appearing as noise. A receiver can be arranged to listen in parallel to a selection of codes. This enables the receiver to operate a priority scheme such that messages of higher priority take precedence over those of lower priority. Thus for example an interrupt message, which arrives sequentially in the conventional LANs can be processed immediately in the spread spectrum network.

As stated above, the present invention uses the concept of code division multiple access (CDMA) involving a trade-off between bandwidth and signal-to-noise for a fixed channel capacity and the sharing of this channel bandwidth between a number of simultaneous users. Time dependent tranmissions as used in other known forms of CDMA are not used. The spectral compression by the receiver correlation process is able to discriminate against impulsive noise and multi-path signals on the network.

The individual point-to-point data rate is given by equation (1),

$$R_d = R_c/(mL) \qquad (1)$$

where R_c is the code sequence rate, m is the number of sequences per data bit, L is the code sequence length and R_d the resulting data rate. The term 'mL' is defined as the process gain. If the number of simultaneous users is K, then the network-wide data throughput (R_{tot}) is given by equation (2), provided all the users transmit with the same R_c, L and m.

$$R_{tot} = KR_c/(mL) \qquad (2)$$

The term (K/mL) is called the 'data definition factor' (DDF). It relates the total number of network users to the number of code bits ('chips') used to define each data bit. In general, the more users that try to access the network the better 'defined' each data bit will have to be to enable the receiver's correlators to pick out the data in the presence of the K-1 other users 'noise' - since in general their code sequences will not correlate well with the sequence in question and so will appear as additive white Gaussian

noise (AWGN). The data definition factor can be redefined as the relationship between the 'efficiency of use of the network' (u) and the ratio of the total number of nodes (N) to the code sequence length (d), as shown in equation (3).

$$DDF=(K/mL)=K/N)(N/L)/m=(ud)/m \qquad (3)$$

where we assume there is only one code per node. Equations (2) and (3) can now be used to provide equation (4).

$$R_{tot}=(ud/m)R_c \qquad (4)$$

It has been shown that the SNR at the output of the correlator is given by equation (5), where SNR_1 is the signal to noise ratio of a single node with no other users, and f(R) is a function of the aperiodic ACF which is dependant on the types of codes employed in the direct sequence spread spectrum modulation.

$$SNR=(((K-1)/f(R))/L+(1/SNR^2)_1)^{-0.5} \qquad (5)$$

This equation must now be altered to account for the hard limiting at the output to the receiver and to include the DDF. The effect of a hard limiter has been shown to give rise to equation (6).

$$SNR=((2udf(R))/(pi\ m) + (1/SNR^2)_1)^{-0.5} \qquad (6)$$

f(R) is dependant on the types of code sequences and for truly random codes (which could not, of course, be used in a real system) this function becomes 1/3. The final form of the multiple user SNR is now given by equation (7),

$$SNR=((2ud)/3\ pi\ m)+(1/SNR^2)_1)^{-0.5} \qquad (7)$$

The quantity SNR is now used in the definition of the probability of error (P_e) and the BER. The probability of error is defined by equation (8) where I is the standard Gaussian cumulative distribution function which provides a good approximation for the real probability of error.

$$P_e=(1-I(SNR)) \qquad (8)$$

Finally the BER is defined by equation (9), where R_d, P_e and BER all refer to point-to-point communications on the network.

$$BER=R_dP_e=Rd(1-I(SNR)) \qquad (9)$$

From the foregoing equations we can calculate the variation in

data throughput, SNR and P_e with DDF, SNR_1 and Rc.

Equation (4) shows that the DDF is inversely proportional to the processing gain and it is usually the case that a higher processing gain permits a larger number of simultaneous users, but at the expense of a lower point-to-point data rate. It is important to note that the DDF is affected by three factors which can be traded off against each other to provide appropriate operating conditions. A larger number of simultaneous users implies more pn chips per data bit which, for given hardware, implies a lower point-to-point data rate. However the sum of all the point-to-point data rates should remain constant, if the network is being used to its full capacity. To achieve a high network data throughput requires all nodes to be active simultaneously - if some of the nodes choose not to transmit data it will lower the overall efficiency since those nodes still operating will not be able to take advantage of the spare bandwidth without changing the network DDF.

In most communication systems the SNR at the output of the receiver improves if the signal level at the transmitter is increased. However in the SS LAN equation (7) can be used to show that there is a limiting effect on the multiple user SNR. This is because the DDF has a limited SNR resolution ability and once that limit is passed no increase in the signal level will improve the receiver output SNR. Where the DDF is 0.1 and 0.01 the thresholds are set at 5dB and 7dB respectively. In addition, it can be shown that the SNR can achieve a value approaching the single user SNR by using a low enough DDF.

The BER and the probability of error are related, as shown in equation (9), by the point-to-point data rate. It can be shown that the advantage to be gained in Pe against SNR from improving the DDF gradually diminishes. Clearly there will be some optimum value to be chosen for the DDF to be used in practice. In addition, the probability of error Pe increases dramatically for a specified SNR_1 as the DDF is worsened. The limiting effect of the probability of error indicates that a value for SNR_1 of greater than 7dB is most desirable.

Thus the equations lead to the following performance guidelines for a realisable SS LAN:

a. The DDF should be in the range 10^{-4} to 10^{-2}.

b. The single user SNR_1 should be in the range 7dB to 10dB which, if coupled with the lower values of DDF, will give a multi-user SNR approaching that of the single user.

c. To keep the efficiency of the network as high as possible all nodes should be transmitting. If this is not the case then the length of the code sequence should be altered so as to reflect the change in the number of active nodes. In general this will lead to a reduction in the length of the pn sequence and a corresponding rise in the bandwidth available to each node, given that the chip rate at each node is fixed.

An SS LAN system functional configuration is shown in Figure 9. Four work-stations 65 are shown. Each work station 65 is composed of four sections: the user devices (66_1-66_3), the Spreadnet Interface Logic (SIL) 67, the Spread Spectrum Node Controller (SSNC) 68 and the Spread Spectrum Asynchronous Receiver and Transmitter (SSART) 69 - the last two forming the Spreadnet Node Logic (SNL) 70. The SIL 67 converts the general SS-LAN interface into a form useable by particular devices and is therefore host device dependent. The SNL 70 module was designed in two sections so that each workstation could be provided with an efficient parallel processing capability while still maintaining a flexible interface. The SSNC 68 is responsible for control of the individual nodes and the overall network management - this includes the distribution of the codes, reconfiguration of the LAN and the logical-to-physical mapping of user requests to SSART 69 availability. The SSART 69 performs the physical transmission and reception of the data, provides low level error detection and correction, and implements the data link level protocols necessary for the individual communication links. Each SSART 69 is a node in the generally accepted definition of the word - hence the various protocol definitions described earlier (unique receiver, unique transmitter) refer to this block. This arrangement allows either a single device 66_1 (eg a database) to communicate with several other devices simultaneously and have unrestricted access to the channel or for several devices eg 66_2 or 66_3 to operate in parallel with unrestricted access to the channel. The number of SSARTs 69 that the SSNC 68 can control simultaneously will

be limited by the processor capability (a 12MHz 68000 system is used). The software in the 68000 system inspects its own physical configuration and from this information performs the mapping of user requests to available SSART's 69.

Figure 10 shows a more detailed view of the SNL 70. The common modular SSNC 68 comprises a microprocessor 71, a ROM 72 containing fixed system information and a RAM 73 for storing programmable system information. A multiplexor 74 is connected between the microprocessor 71 and an input/output connection 75 to a SIL 67 for each device. Each multiplexor 74 is also connected to an input/output connection 76 for connection to respective SSARTs 69. Each SSART 69 includes a microprocessor 77 connected to a RAM 78 and a ROM 79 and a transmitter 80 and receiver 81. The transmitter is connected to the LAN via an amplifier 82 to launch the binary coded spread spectrum signal. The physical transmission of the signal is either by a raised cosine pulse for a co-axial cable medium or directly by means of optical fibres. The receiver 81 has a hard limiter 83 at its input to convert the signal on the LAN to a binary form.

Considering first the operation of the SSNC 68. All requests for the establishment of virtual communications links must be received by the SSNC-CPU 71. This will in turn either allocate a free SSART 69 or, should none be available, queue the request and inform the host. The SSNC 68 can also request its own virtual link - this is necessary when network management information must be circulated to other SSNC's. The SSNC-RAM 73 contains the updated code distribution mapping tables, the SNL activity tables and other general SNL and network wide housekeeping information. At initialisation the SSNC 68 is responsible for the self-testing of the SNL's, followed by the current status of the network. It then announces the presence of the newly available nodes to the rest of the network and gathers appropriate information regarding the codes in use and the time. Similarly, at power down, the SSNC 68 informs all other SSNC's of its controlled termination in an attempt to leave the other SSNC's with an accurate and consistant image of the network configuration.

Once a data transfer request has been received by the SSNC 68,

it allocates and primes an appropriate SSART 69. The SSART 69 requests the code generation parameters from the SSNC-CPU 71 and stores them in the SSART-RAM 78. Either the transmitter or receiver will be activated and the appropriate code sequence is taken from the RAM 78 and stored in either the correlators (receive function) or the encryptors (transmit function). In many cases this information may already be available in local RAM associated with either the correlators or the encryptors - since the SSNC 68 is arranged such that it attempts to predict the next code sequences to be used and stores them in a code cache. These codes may then be accessed by simple pointer operation - no actual transfer of code data being needed - thus speeding the access time. Actual modulation of the data to be transmitted, or demodulation of the received data, is handled by dedicated hardware (a custom-programmed logic array), leaving the SSART-CPU 77 free to co-ordinate further data transfers.

The transmitter operates at a code sequence rate of 12 MHz with a fixed sequence length of 127 bits using linear codes. Figure 11 is a schematic diagram of this receiver hardware. The heart of the receiver is a pair of TRW 64-bit correlator-chips 84 connected in series. These devices each contain two 64-bit shift registers, the appropriate exclusive-OR gates and a high speed look-ahead adder (to generate the correlation coefficient). In operation the SSNC 68 loads the upper correlator shift register via a field programmable logic array (FPLA) 85 with a copy of the pn sequence for which the receiver wishes to search. After this has been done, the FPLA control logic allows data 86 from the network via a sampling circuit 87 and a limiter 88 into the correlator 84. As this data 86 is 'clocked through' the correlator 84 it effectively slides past the resident sequence. At each clock period the look-ahead adder computes the correlation coefficient between the resident sequence and the sliding sequence. In general the two sequences will not be in step and so the correlation coefficient will be low. However, eventually the output from the look-ahead adder will exceed the threshold of a programmable threshold detector 90 to indicate that the sequences are in step and will show either a maximum (data was logic '1') or a minimum (data was logic '0'). This data is assembled into 16-bit words by the FPLA (85) control logic and then

placed into a buffer 89 where the SSNC 68 is able to access it via the FPLA 85.

If we assume that each node on the network is able to generate either zero volts (to represent a logic '0') or one volt (to represent a logic '1') then the voltage on the network will vary between zero and n volts, where n is the current number of users. The sampling circuit 87 operates in real time to derive an appropriate threshold for the limiter 88 such that the data is converted to a binary form suitable for connection to the correlator 84. Extensive simulations have shown that the correlation threshold of the detector 90 must be changed in real time since the correlation coefficient between two identical sequences falls off relative to the background noise as the number of users increases. This task is also handled by the SSNC 68 via the FPLA 85. The sampling circuit 87 is arranged to over-sample the incoming data 86 to derive time signals to synchronise the correlator clocks with the incoming data.

In general, in any LAN, there are many more nodes connected to the medium than are trying to communicate at any one moment. In the present system there is a relationship between the medium bandwidth available, the maximum number of nodes able to transmit simultaneously and the data rate as discussed earlier. If a large number of nodes wish to transmit simultaneously then the bandwidth available to each will be relatively small. In order to effectively utilise the available medium bandwidth each node must employ a long pn sequence - this also facilitates the recovery of that node's signal from amongst the large number of other signals. If only a small number of nodes wish to use the network they have access to a correspondingly larger bandwidth each and so only a short pn sequence will be required. In situations where the network load is likely to fluctuate it will be necessary to perform dynamic mapping of the pn codes used onto the physical addresses. This can have other related advantages. In situations where the number of simultaneous users is much less than the total population of nodes, it may be difficult to find sufficient pn codes to allocate to every potential user. In this case a 'code pool' must be used, with nodes attaching and releasing codes as necessary. Clearly this also has

the side benefit of increasing security - to obtain illegal access to the network, or to 'spoof' a terminal attached to it, will require a dynamic tracking of the codes used. Code distribution may be via a cryptographic technique to prevent unauthorised code tracking.

Since each node in the spread spectrum network has the capability of receiving and decoding multiple data streams simultaneously it is arranged to allocate one channel per node for handling channel management functions. Each node makes known its own code and determines the current usage of pn codes on the network via this channel. Before a node establishes a code for use on the network it monitors the network to see whether or not such a code is currently in use. This can be achieved by rapidly loading the local correlator with a copy of the code being tested and by observing whether or not there is significant correlation. If the code is not currently in use then its value may be communicated to the intended destination node by means of the cryptographic system mentioned earlier. Subsequent data exchanges may take place with no access delay.

The management channel is used to perform real-time updating of the pn sequences in use on any virtual link. This significantly improves the security of the system and also allows the network to adapt dynamically to load changes. If a node finds that a queue of data is waiting to be sent over the network, then it will attempt to increase the rate at which it is sending the data by shortening the pn sequence being used. This can only be accomplished if the number of nodes currently using the system is below a critical level which each node is constantly monitoring. Similarly, when the loading of the network increases beyond some predetermined limit, a node may find that it is required to lengthen the code sequence that it is currently using in order to be able to operate in the deteriorating signal-to-noise environment. This in turn will require that node to reduce its data rate and consequently a queue of data may start to build up at a node. If the usage of the network should subsequently reduce then nodes will be able to increase their data rate proportionally. In order to perform real-time code updating, each receiver must maintain at least one free code channel that can be

made available to management functions. This ensures that a smooth changeover can be made from the old pn sequence to the new with no loss of data or comprising of the system integrity. To perform the update function the transmitter informs the receiver of the new code to be employed by use of the techniques already described. The receiver then loads the new pn code into a spare channel and waits for the data being received by the old pn sequence to finish. Simultaneously it should start to receive data on the new channel. The use of the spare channel avoids the problems associated with the finite time required to load the correlators with a new sequence and avoids any reduction in the date throughput while code changeover occurs. Such changeovers are co-ordinated by the management software, and only one spare channel is needed per node - irrespective of the number of parallel data channels that node contains. For non-critical data channels, or for times when hardware failures have removed spare channel capacity, the node management is also able to effect a code chaneover, albeit with a small delay while the code is loaded into the correlator. In this case the receiver monitors the data on the 'old' channel. When this data terminates, it simply reloads the correlators with the new pn sequence and continues demodulation of the data. The transmitter is made aware of this situation (via the network management) and allows sufficient time, after pn code changeover, for the receiver to re-load its correlators with the new sequence. This is because, at the transmitter, the SSNC only needs to perform a pointer change in the SSART RAM to effect the code change. This is handled by the FPLA logic controlling the SSART and can occur within a chip period - thus there is no pause whatsoever as the code changeover occurs. If the receiver cannot handle this situation (because it has no spare channel) then the SSNC calculates how long it will require the receiver to change over codes (it knows the new code length and so can easily calculate this time) and will instruct the FPLA to place a delay in the code changeover.

The present invention has been described in relation to direct sequence linear code sequences. Other sequences having the appropriate correlation properties may be employed. Other modifications of the embodiments described will be apparent to those skilled in

the art, all falling within the scope of the present invention. Because of its good immunity to medium interference (multipath and impulsive noise) the spread spectrum LAN is suitable, for example, for use in domestic control systems interconnected via the electric mains. The system could also be used for remote reading of domestic or other meters via the mains.

Claims

1. A serial data local area network system comprising a serial data highway 10 interconnecting a plurality of transmitting/receiving nodes having transmitters and/or receivers 12 connected thereto characterised in that each transmitter includes means 22, 23 to spread-spectrum modulate digital data signals 21 and address said data signals and means 24 to connect the baseband modulated signal to the highway and each receiver includes means 26 - 29 to selectively demodulate the respective addressed signals from the received signal to reconstitute the data signals, the arrangement being such that multiple simultaneous data signals can be connected to the highway.

2. A serial data network system as claimed in claim 1 wherein the spread-spectrum modulation means comprises a pseudo-random binary generator 23 and an adder 22 connected such that each data signal is modulo-2 added to a pseudo-random binary number sequence.

3. A serial data network system as claimed in claim 1 or 2 wherein bipolar signalling is used such that a positive voltage represents a logical "1" and a negative voltage represents a logical "0".

4. A serial data network system as claimed in claim 2 or 3 wherein each appropriate receiver includes a local pseudo-random binary number sequence generator 27 for generating a sequence identical to the transmitted spread-spectrum modulation sequence and synchronised thereto to demodulate the transmitted data.

5. A serial data network system as claimed in any one of claims 2 to 4 wherein the pseudo-random binary sequence is one selected from a plurality of orthogonal pseudo-random number sequences, each number sequence serving to characterise a required transmission such that simultaneous transmissions can occur on the network without mutual interference.

6. A serial data network as claimed in any one preceding claim wherein the codes are generated by a maximal length code generator (m-sequences).

7. A serial data network as claimed in claim 6 wherein data bits 43 are synchronised to the pseudo-random binary sequence 45 by detecting the all "1"s state 46 of the m-sequence generator and starting a data bit at that time.

8. A serial data network system as claimed in claim 7 including a cyclic counter 47 which is periodically used to determine the start of subsequent data bits.

9. A serial data network as claimed in any one preceding claim wherein each receiver includes means 58, 109 to convert the received signal into a binary signal.

10. A serial data network as claimed in claim 9 wherein the binary converting means comprises a 1-bit analog to digital (A/D) converter 109 producing a logical "1" or "0" in dependence on whether the received signal is positive or negative respectively.

11. A serial data network as claimed in claim 10 wherein local receiver clock timing is synchronised with the received spread spectrum signal by oversampling 110, 113 the signal to derive the required timing information.

12. A serial data network as claimed in claim 11 wherein the received signal is sampled at twice the nominal sequence rate and majority voting 113 is used over three consecutive sampling periods to determine the binary signal information without initial synchronisation.

13. A serial data network as claimed in any one of claims 5 to 8 wherein a receiver is provided with a stack 53 of the pseudo-random number (pn) sequences and a sliding polarity receiver correlator 114 constantly searches serially for correlations of the received signal with the local pn sequences in the stack.

14. A serial data network as claimed in claim 13 wherein the correlator output is connected to a demodulator 62 arranged such that when the correlator determines that a transmitted pn

sequence is present in the received signal and in phase with one of the locally generated pn sequences, the demodulator then decodes the signal data.

15. A serial data network as claimed in claim 14 wherein a threshold detector 90 is connected to the correlator output.

16. A serial data network as claimed in claim 15 wherein the correlator 114 compares the local pn sequence with the received binary converted signal by counting the number of agreements (A) or disagreements (D) over the entire sequence length (L) then calculating the value (V) of (A-D)/L (117) and comparing V to two threshold values (118) selected such that a logical "1" is produced if V lies between the two thresholds and a logical "0" is produced if V exceeds the upper threshold.

17. A serial data network as claimed in claim 15 or 16 wherein an adaptive threshold detector 58 is used, there being included means 57 to determine the number of active users on the network and the threshold level being adjusted in dependence upon the number of users.

18. A serial data network as claimed in claim 9 wherein the received signal is connected to an n-bit analog to digital (A/D) converter 109, n correlators are used to correlate the binary signals from the different n bits in the output from the A/D converter, and the correlator outputs are combined using weighting factors according to the significance of the n bits to thereby obtain the data bit.

19. A serial data network as claimed in any one preceding claim wherein the data definition factor - the ratio of the number of simultaneous users to the number of code bits used to define each data bit - is in the range 10^{-4} to 10^{-2}.

20. A serial data network as claimed in any one preceding claim wherein the signal-to-noise ratio of a single node in the absence of other users is in the range 7dB to 10dB.

21. A serial data network as claimed in any one of claims 5 to 20 including means to change the length of each pn sequence in dependence on the number of active users.

22. A serial data network as claimed in any one of claims 5 to 21 wherein receivers are adapted for parallel decoding such that more than one pn sequence can be decoded simultaneously.

23. A serial data network as claimed in any one of claims 5 to 22 wherein a priority is assigned to at least one preselected pn sequence.

24. A serial data network as claimed in any one of claims 13 to 23 wherein the local pn sequence generator is driven by an accurately controlled frequency source such that once the correlator detects the appropriate incoming pn code-modulated signal the correlator is no longer required to track the incoming spread-spectrum sequence and can continue searching the stack of code sequences.

Fig.1.

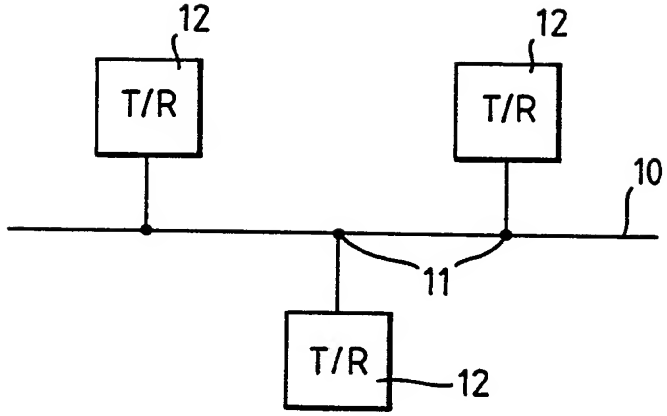

12
12
T/R
T/R
10
11
T/R
12

Fig.2.

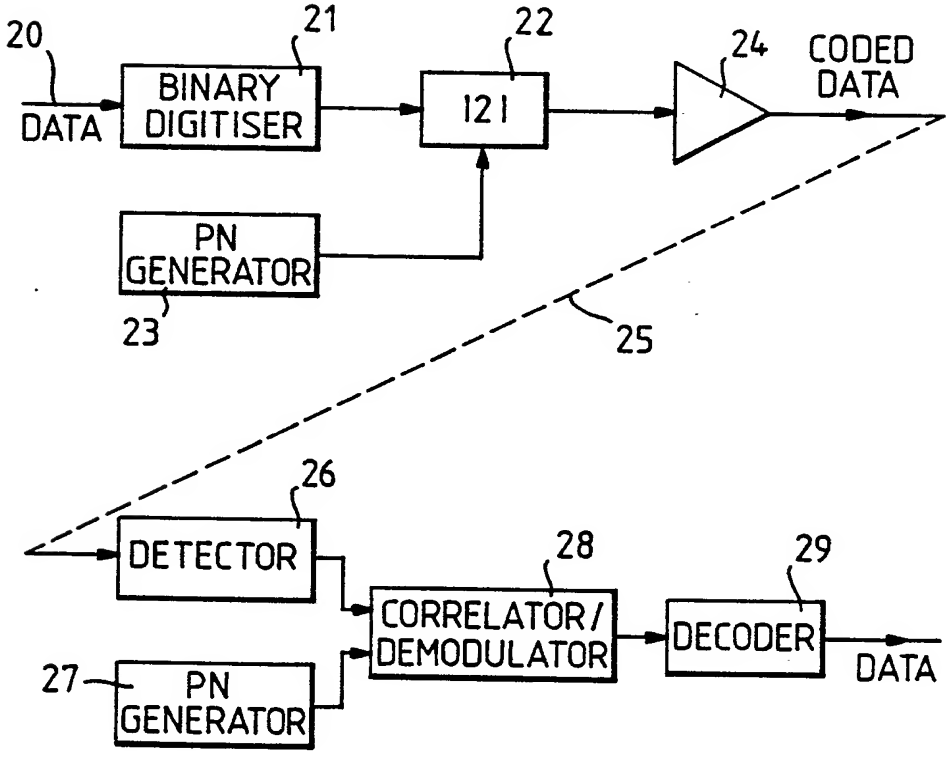

20
DATA
21
BINARY DIGITISER
22
121
24
CODED DATA
PN GENERATOR
23
25
26
DETECTOR
28
CORRELATOR/ DEMODULATOR
29
DECODER
DATA
27
PN GENERATOR

Fig. 3.

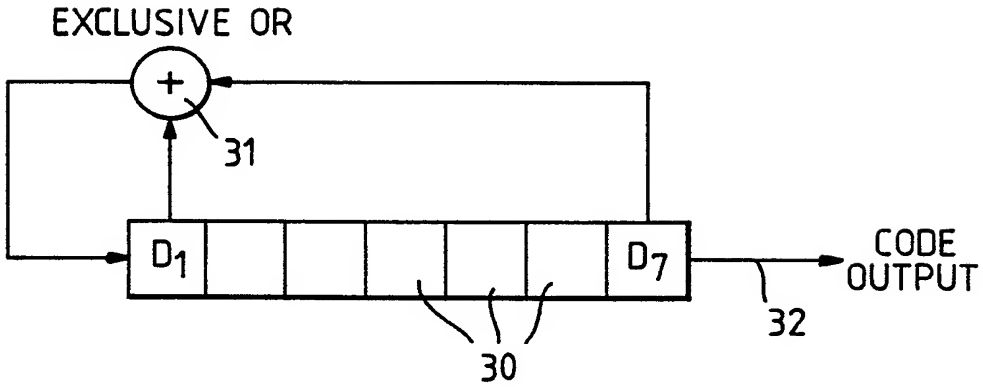

EXCLUSIVE OR
+
31
D1
D7
CODE
OUTPUT
32
30

Fig. 4.

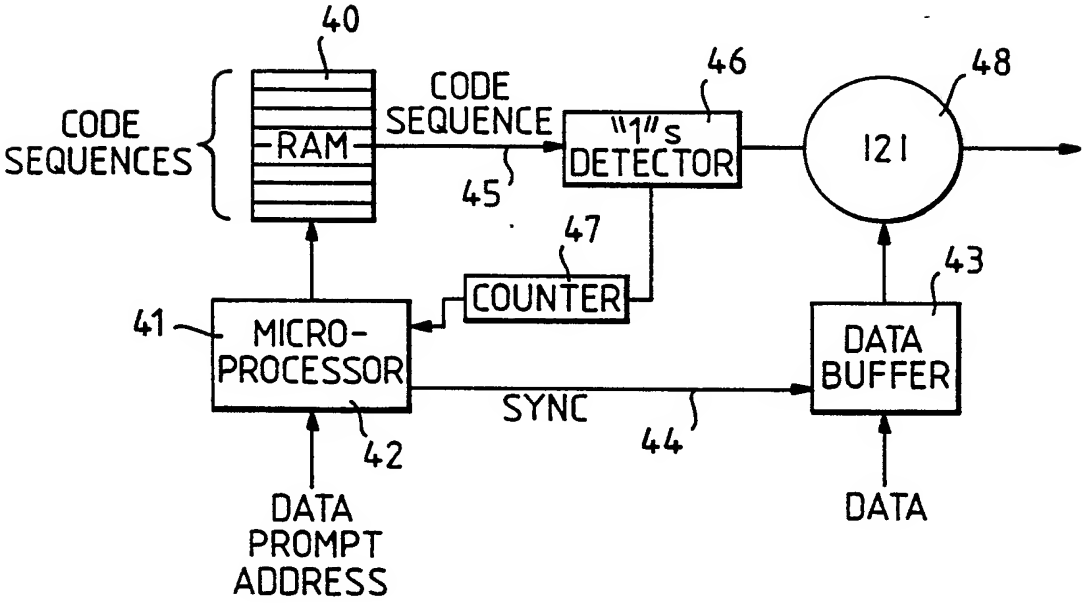

40
CODE
SEQUENCES
RAM
CODE
SEQUENCE
45
46
"1"s
DETECTOR
48
121
47
COUNTER
43
41
MICRO-
PROCESSOR
DATA
BUFFER
SYNC
44
42
DATA
PROMPT
ADDRESS
DATA

Fig.5.

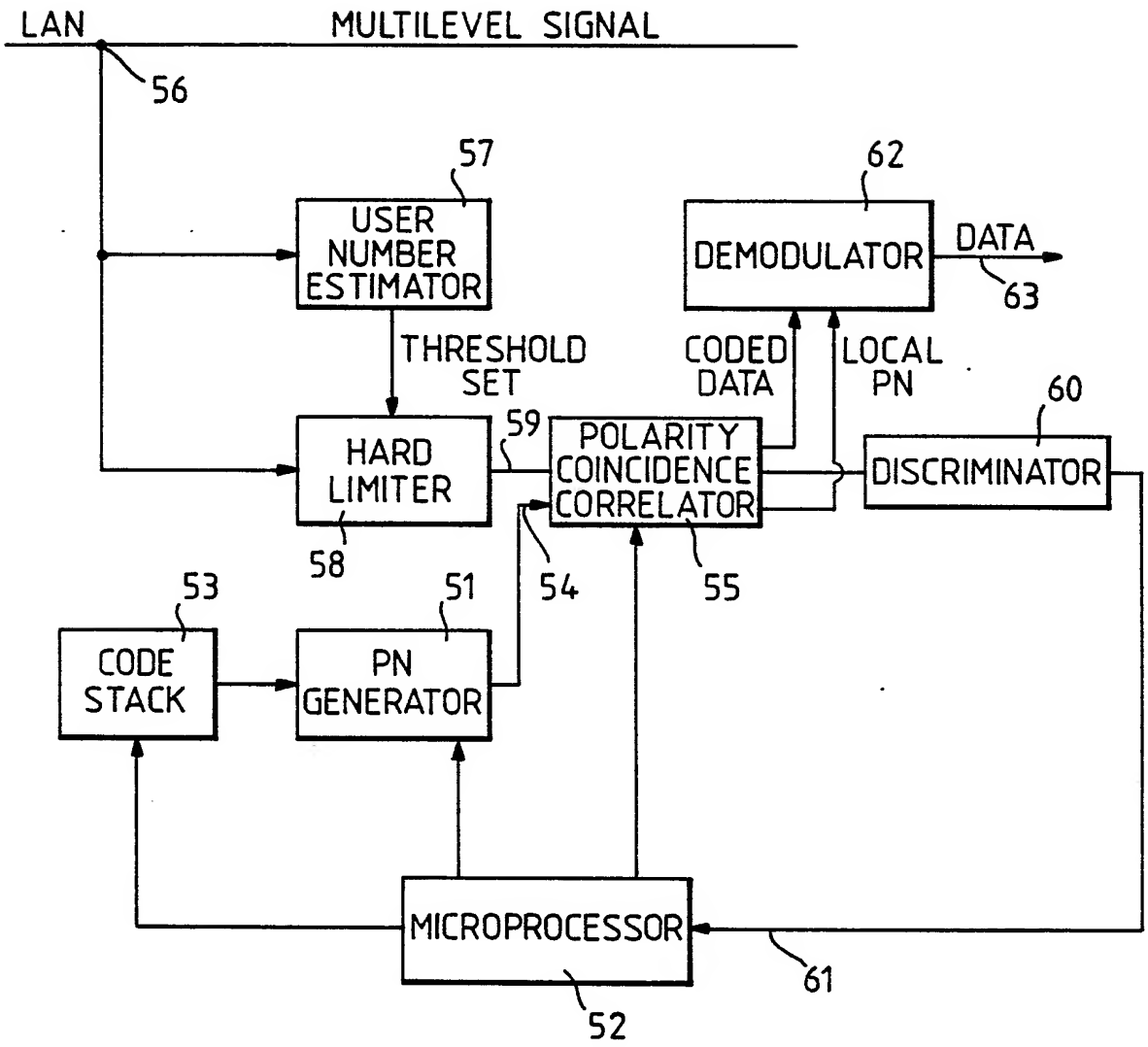

LAN
MULTILEVEL SIGNAL
56
57
USER NUMBER ESTIMATOR
62
DEMODULATOR
DATA
63
THRESHOLD SET
CODED DATA
LOCAL PN
60
59
HARD LIMITER
POLARITY COINCIDENCE CORRELATOR
DISCRIMINATOR
58
54
55
53
51
CODE STACK
PN GENERATOR
MICROPROCESSOR
61
52

Fig.6.

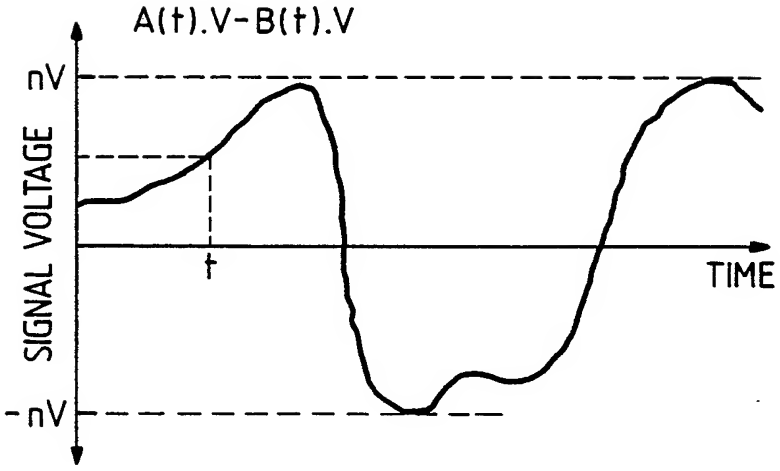

A(t).V-B(t).V
nV
SIGNAL VOLTAGE
t
TIME
-nV

Fig.8.

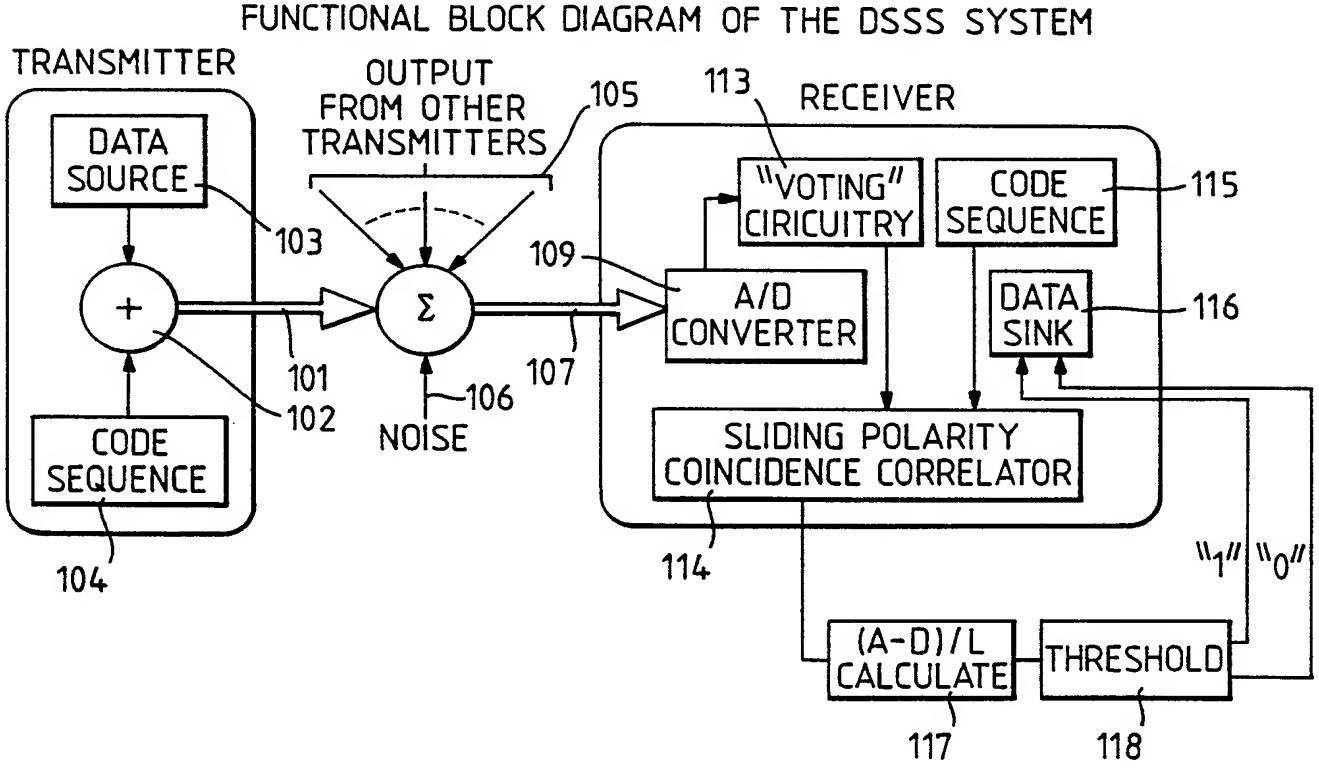

FUNCTIONAL BLOCK DIAGRAM OF THE DSSS SYSTEM
TRANSMITTER
DATA SOURCE
103
+
101
102
CODE SEQUENCE
104
OUTPUT FROM OTHER TRANSMITTERS
105
Σ
106
NOISE
107
109
113
RECEIVER
"VOTING" CIRICUITRY
CODE SEQUENCE
115
A/D CONVERTER
DATA SINK
116
SLIDING POLARITY COINCIDENCE CORRELATOR
114
"1" "0"
(A-D)/L CALCULATE
117
THRESHOLD
118

Fig.7a)

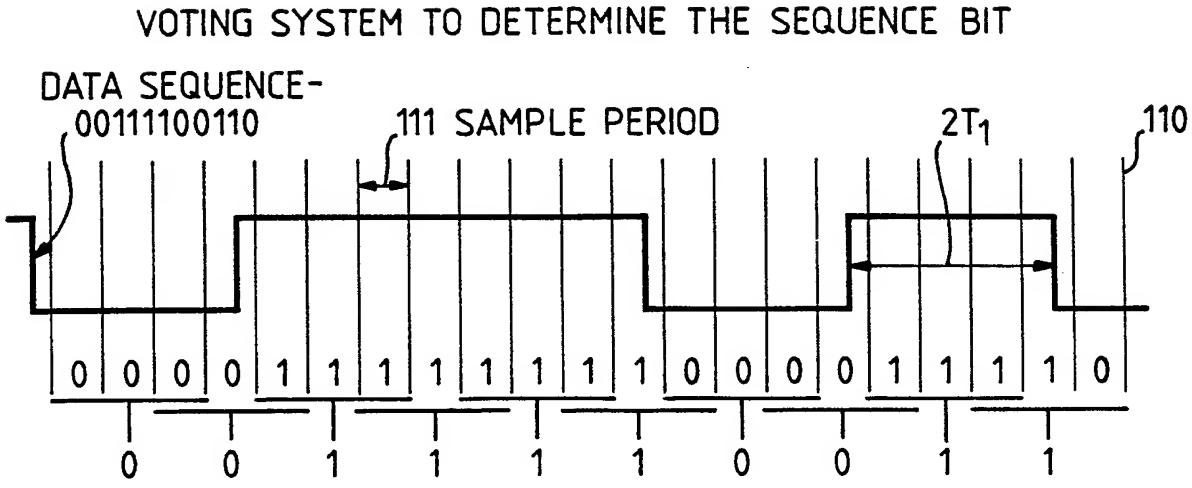
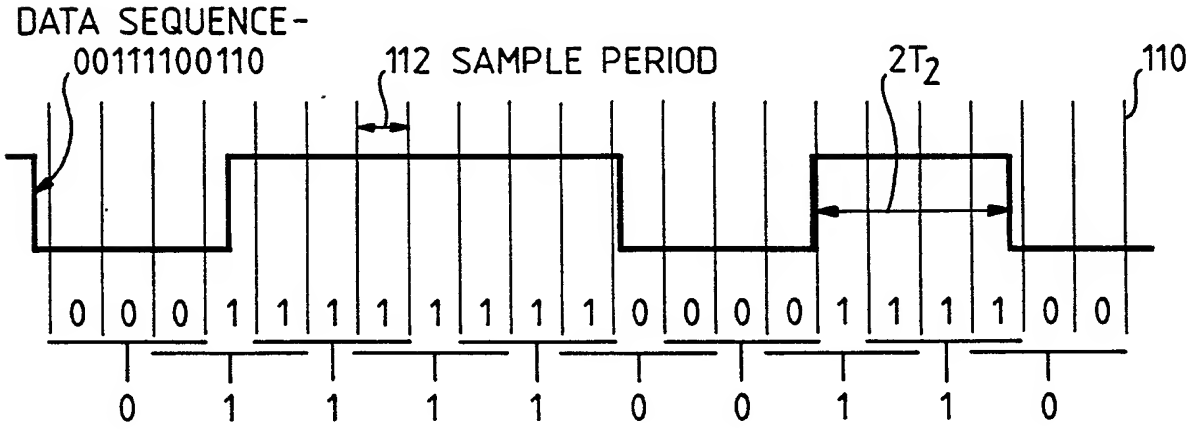

VOTING SYSTEM TO DETERMINE THE SEQUENCE BIT
DATA SEQUENCE-
00111100110
111 SAMPLE PERIOD
2T1
110
0 0 0 0 1 1 1 1 1 1 1 1 0 0 0 0 1 1 1 1 0
0 0 1 1 1 1 0 0 1 1

Fig.7b)


VOTING SYSTEM TO DETERMINE SEQUENCE BIT
DATA SEQUENCE-
00111100110
112 SAMPLE PERIOD
2T2
110
0 0 0 1 1 1 1 1 1 1 1 0 0 0 0 1 1 1 1 0 0
0 1 1 1 1 0 0 1 1 0

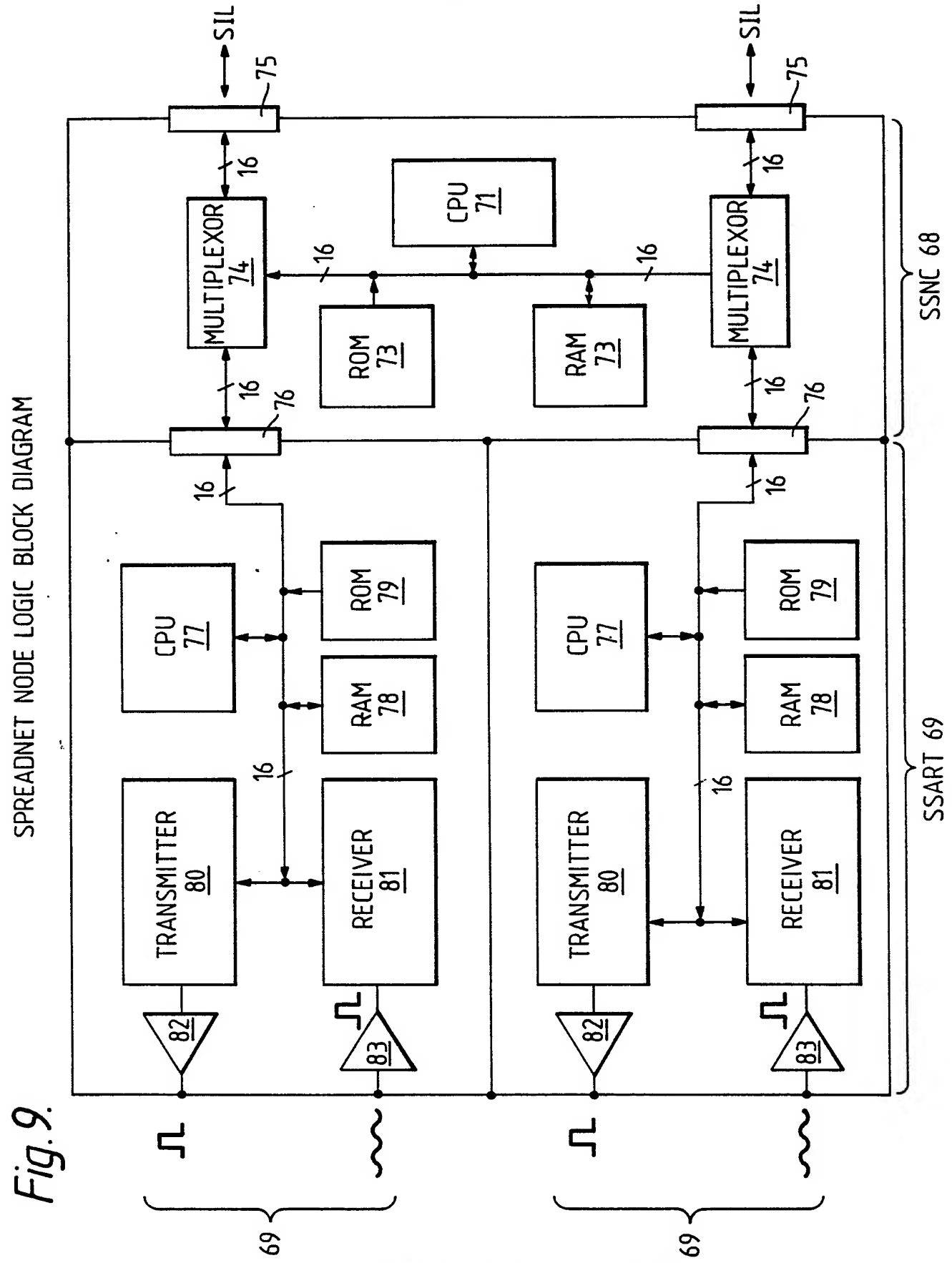

SPREADNET NODE LOGIC BLOCK DIAGRAM
SIL
75
16
MULTIPLEXOR 74
CPU 71
ROM 73
RAM 73
76
SSNC 68
CPU 77
ROM 79
RAM 78
TRANSMITTER 80
RECEIVER 81
82
83
SSART 69
69

Fig. 9.

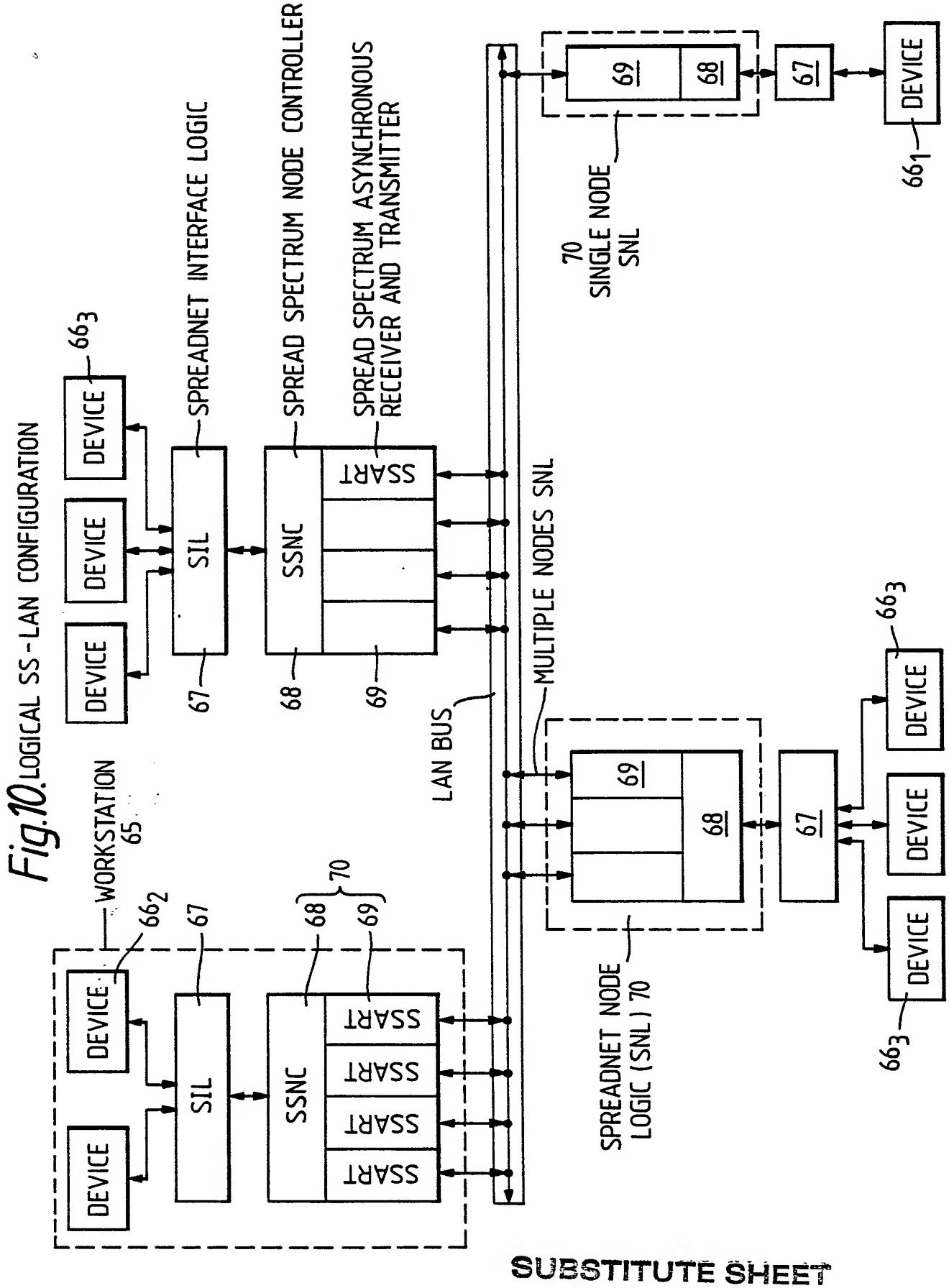
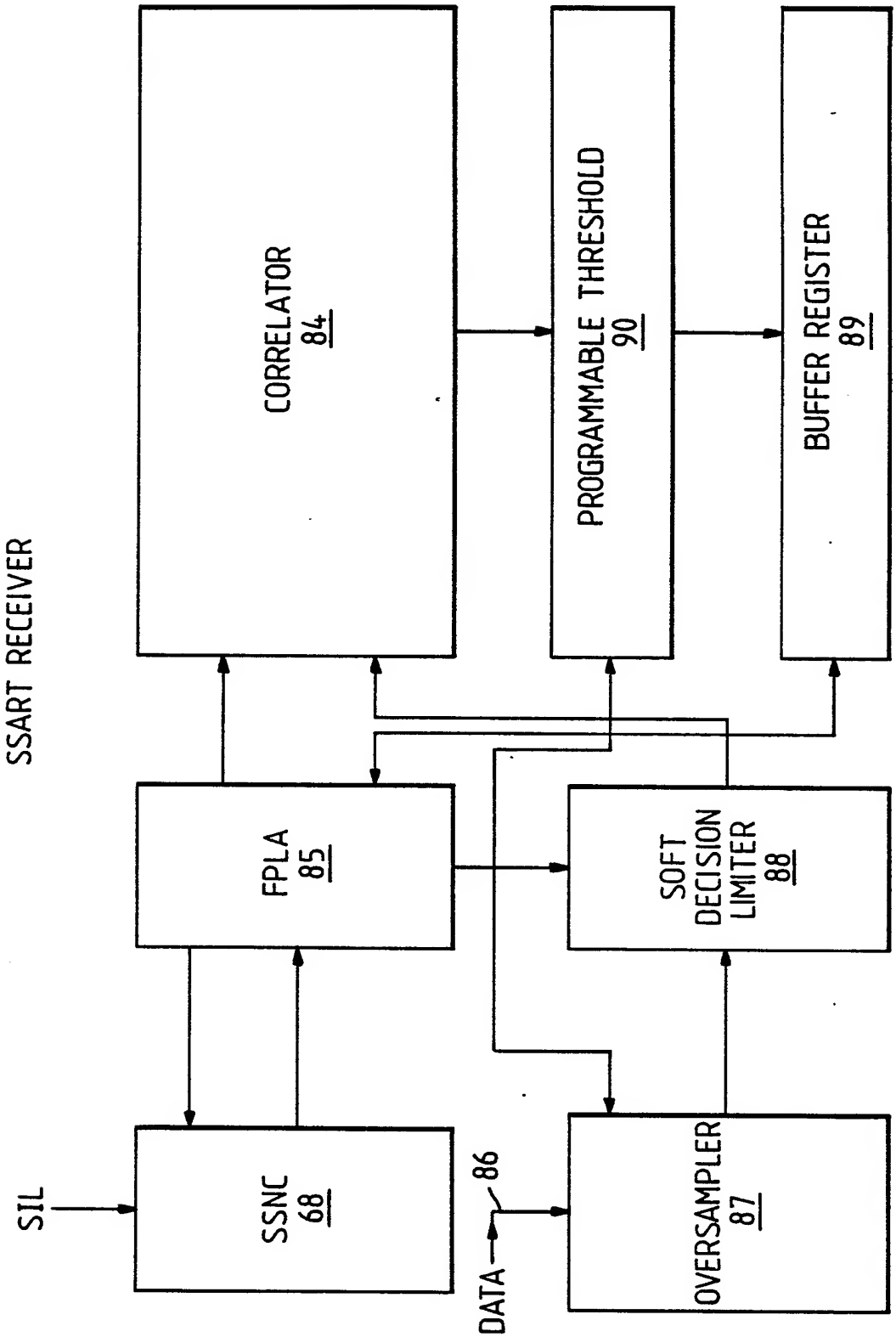


Fig.10. LOGICAL SS-LAN CONFIGURATION

Fig. 11.


SSART RECEIVER
CORRELATOR
84
PROGRAMMABLE THRESHOLD
90
BUFFER REGISTER
89
FPLA
85
SOFT
DECISION
LIMITER
88
SSNC
68
OVERSAMPLER
87
SIL
DATA
86

INTERNATIONAL SEARCH REPORT

International Application No PCT/GB 86/00372

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: H 04 J 13/00

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	H 04 J H 04 B

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	IEEE National Telecommunications Conference, New Orleans , Louisiana, 29 November - 3 December 1981, (New York, US), Hirosaki et al.: "Spread-spectrum Multiple access data loop", pages G8.5.1 - G8.5.6 see page G8.5.1, left-hand column, line 28 - right-hand column, line 13; page G8.5.2, left-hand column, line 36 - right-hand column, line 5	1,2,4,6,9
X	Electroncis and Communications in Japan, volume 65, no. 9, September 1982, (Silver Spring, Maryland, US), SUGIYAMA et al.: "A method for increasing number of co-channel users in spread spectrum multiple access communication systems", pages 29-37 see page 30, left-hand column, line 1 - right-hand column, line 14; page 36, left-hand column, line 34 - page 37, left-hand column, line 25	1,2,4,6
A		19-21,24

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
3rd October 1986	14 NOV 1986
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL